Notice of References Cited	Application/Control No. 09/954,715	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,663,900	09-1997	Bhandari et al.	716/17
	B	US-5,661,662	08-1997	Butts et al.	716/16
	C	US-6,212,489	04-2001	Klein et al.	703/13
	D	US-6,223,144	04-2001	Barnett et al.	703/22
	E	US-6,202,044	03-2001	Tzori, Yiftach	703/28
	F	US-6,188,975	02-2001	Gay, Donald L.	703/22
	G	US-6,182,247	01-2001	Herrmann et al.	714/39
	H	US-6,075,935	06-2000	Ussery et al.	716/17
	I	US-6,766,284	07-2004	Finch, Peter	703/20
	J	US-6,356,862	03-2002	Bailey, Brian	703/16
	K	US-6,304,903	10-2001	Ward, Robert G.	709/224
	L	US-6,298,320	10-2001	Buckmaster et al.	703/28
	M	US-6,286,114	09-2001	Veenstra et al.	714/39

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Q-modules: internally clocked delay-insensitive modules"; Rosenberger, F.U. et al; Computers, IEEE Transactions on Volume 37,Issue 9,Sept. 1988 Page(s):1005 - 1018
	V	"A heterogeneous environment for hardware/software cosimulation"; Bishop, W:D. et al; Simulation Symposium, 1997. Proceedings. 30th Annual 7-9 April 1997 Page(s):14 - 22
	W	"High speed externally asynchronous/internally clocked systems"; VanScheik, W.S. et al; Computers, IEEE Transactions on Volume 46, Issue 7, July 1997 Page(s):824 - 829
	X	IEEE Std 1275.2-1994: IEEE Standard for Boot (Initialization Configuration) Firmware: Bus Supplement for IEEE 1496 (SBus)

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/954,715	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,223,144	04-2001	Barnett et al.	703/22
	B	US-6,052,524	04-2000	Pauna, Mark R.	703/22
	C	US-5,937,179	08-1999	Swoboda, Gary L.	716/16
	D	US-5,911,059	06-1999	Profit, Jr., Jack H.	703/23
	E	US-5,838,948	11-1998	Bunza, Geoffrey J.	703/27
	F	US-5,815,688	09-1998	Averill, Gregory S.	716/4
	G	US-5,684,721	11-1997	Swoboda et al.	703/23
	H	US-5,603,043	02-1997	Taylor et al.	712/1
	I	US-5,572,437	11-1996	Rostoker et al.	716/18
	J	US-5,546,562	08-1996	Patel, Chandresh	703/14
	K	US-5,363,501	11-1994	Pullela, Somayajulu S. K.	703/20
	L	US-5,329,471	07-1994	Swoboda et al.	703/23
	M	US-5,109,353	04-1992	Sample et al.	716/17

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE Std 1364-1995: IEEE Standard Hardware Description Language Based on the Verilog Hardware Description Language; Pg.101 w/comments
	V	IEEE Std 1364-1995: IEEE Standard Hardware Description Language Based on the Verilog Hardware Description Language; Pgs.370-371
	W	Prior Art from U.S. Patent 5808486 on the edge detector 1997.
	X	"An SBus Monitor Board"; Xie, H.A. et al; Field-Programmable Gate Arrays, 1995. FPGA '95. Proceedings of the Third International ACM Symposium on 1995 Page(s):160 - 167 □□

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/954,715	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,259,006	11-1993	Price et al.	375/356
	B	US-6,836,877	12-2004	Dupenloup, Guy	716/18
	C	US-6,691,268	02-2004	Chin, Douglas	714/726
	D	US-6,169,422	01-2001	Harris et al.	326/98
	E	US-6,108,494	08-2000	Eisenhofer et al.	703/14
	F	US-6,094,532	07-2000	Acton et al.	712/28
	G	US-5,970,240	10-1999	Chen et al.	703/25
	H	US-5,968,161	10-1999	Southgate, Timothy James	712/37
	I	US-5,905,883	05-1999	Kasuya, Atsushi	703/17
	J	US-5,808,486	09-1998	Smiley, David Alan	327/34
	K	US-5,539,330	07-1996	McDermid, William J.	326/39
	L	US-5,387,802	02-1995	Chen et al.	250/551
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A hardware-software co-simulator for embedded system design and debugging"; Ghosh, A. et al; Design Automation Conference, 1995. Proceedings of the ASP-DAC '95/CHDL '95/VLSI '95., Page(s):155 - 164
	V	"AnyBoard: an FPGA-based, reconfigurable system"; Van den Bout, D.E. et al; Design & Test of Computers, IEEE Volume 9, Issue 3, Sept. 1992 Page(s):21 - 30 □□
	W	"The design of RPM: an FPGA-based multiprocessor emulator"; Koray Öner; February 1995 Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays
	X	"Resolution of dynamic memory allocation and pointers for the behavioral synthesis from C"; Semeria, L. et al; Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings 27-30 March 2000 Page(s):312 - 319□□

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.